

METHOD OF FORMING METAL-INSULATOR-METAL (MIM) CAPACITORS

AT COPPER PROCESS

FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication and more specifically to the formation of metal-insulator-metal (MIM) capacitors.

BACKGROUND OF THE INVENTION

With conventional metal-insulator-metal (MIM) processes, there are poor planarization issues at the copper (Cu) area and low-dielectric constant (low-k) damage issues. A low-k damage and loss issue also occurs during ash for the polymer removal and photoresist strip.

U.S. Patent No. 6,528,384 B2 to Beckmann et al. describes a method for manufacturing a trench capacitor.

U.S. Patent No. 6,495,874 B1 to Kawamura et al. describes a semiconductor device and production process thereof.

U.S. Patent No. 6,384,442 B1 to Chen describes a fabrication process for metal-insulator-metal capacitor with low gate resistance.

U.S. Patent No. 6,346,454 B1 to Sung et al. describes a method of making dual damascene interconnect structure and metal electrode capacitor.

SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide an improved method of forming MIM capacitors, and the MIM capacitors formed thereby.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure having a metal structure formed thereover is provided. A dielectric layer is formed over the metal structure and a top layer is formed over the dielectric layer. A capacitance trench is formed through the top layer and into the dielectric layer. Respective bottom electrodes are formed over the opposing side walls of the capacitance trench. A capacitance dielectric layer is formed over: the respective bottom electrodes; the bottom of the capacitance trench; and the remaining top layer. Respective opposing initial via openings are formed adjacent the capacitance trench. Respective trench openings are formed above, continuous and contiguous with the lower portions of the respective opposing initial via openings and exposing portions of the underlying metal structure to form respective opposing dual damascene openings. Planarized metal portions are formed within: the dual damascene openings; and the capacitance trench to form a top electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 12 schematically illustrate a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Information Known to the Inventors - Not to be Considered Prior Art

The inventors have discovered that the reason for the poor planarization issues at the copper (Cu) area and low-dielectric constant (low-k) damage issues are because in the conventional MIM process, a high step height is formed which will make the lower via etching process window to both connect the top electrode and the metal layer.

In the present invention, the capacitance trench 25 and bottom electrodes 30', 30" therein are formed before the trench openings 56, 58 and final via openings 52, 54 are formed.

Initial Structure - Fig. 1

As shown in Fig 1, structure 10 includes metal structure 12 formed thereover to a thickness of preferably from about 100 to 500Å and more preferably from about 200 to 400Å.

Structure 10 is preferably a silicon or germanium substrate and is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers and dielectric layers

(e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer.

Metal structure 12 is preferably comprised of copper (Cu), aluminum (Al) or gold (Au) and is more preferably copper (Cu) as will be used for illustrative purposes hereafter. Metal structure 12 has a thickness of preferably from about 1000 to 9000Å and more preferably from about 2000 to 8000 Å.

An etch stop layer 14 is formed over copper structure 12 to a thickness of preferably from about 300 to 900Å and more preferably from about 400 to 600Å. Etch stop layer 14 is preferably comprised of silicon nitride (SiN) or silicon carbide (SiC).

A dielectric layer 16 is formed over etch stop layer 14 to a thickness of preferably from about 2000 to 12,000Å and more preferably from about 7000 to 9000Å. Dielectric layer 16 is preferably a low-k material such as oxide, silicon oxide or FSG and is more preferably a low-k oxide material as will be used for illustrative purposes hereafter. For the purposes of this invention, low-k means a dielectric constant of less than about 3.0.

A top layer 18 is formed over oxide layer 16 to a thickness of preferably from about 300 to 1500Å and more preferably from about 1000 to

14,000Å. Top layer 18 is preferably an anti-reflective coating (ARC) 18 (as will be used for illustrative purposes hereafter) comprised of silicon oxynitride (SiON).

A first patterned masking layer 20 is formed over ARC 18 and includes opening 22 exposing a portion 24 of ARC 18. First patterned masking layer 20 is preferably comprised of photoresist as will be used for illustrative purposes hereafter.

Formation of Capacitance Trench 25 - Fig. 2

As shown in Fig. 2, using first patterned photoresist layer 20 as a mask, the exposed portion 24 of ARC 18 and a portion of the underlying oxide layer 16 are removed to define a capacitance trench 25 having side walls 26 and a bottom 28. The exposed portion 24 of ARC 18 and the portion of oxide layer 16 are removed preferably using an oxide etch process. It is noted that an etch stop layer (not shown) may be formed within oxide layer 16 to which the oxide etch process etches down to in defining the capacitance trench 25.

Capacitance trench 25 has a width of preferably from about 0.10 to 1.00 μm and more preferably from about 0.20 to 0.40 μm and has a depth of preferably from about 1000 to 9000Å and more preferably from about 2000 to 6000Å.

Formation of Bottom Electrode Layer 30 - Fig. 3

As shown in Fig. 3, the first patterned masking layer 20 is removed from the structure of Fig. 2 and the structure is cleaned as necessary.

Then a bottom electrode layer 30 is formed over the patterned oxide layer 16' the capacitance trench side walls 26 and the capacitance trench bottom 28 to a thickness of preferably from about 100 to 500Å and more preferably from about 200 to 400Å. Bottom electrode layer 30 is preferably comprised of TaN or TiN and is more preferably TaN.

Anisotropic Etching of Bottom Electrode Layer 30 to Form Bottom Electrodes 30', 30'' - Fig. 4

As shown in Fig. 4, an anisotropic etch is performed to remove the horizontal portions of the bottom electrode layer 30 and forming respective bottom electrodes 30', 30'' over the opposing side walls 26 of the capacitance trench 25 leaving exposed a smaller portion of the bottom 28 of the capacitance trench.

Formation of Capacitance Dielectric Layer 32 - Fig. 5

As shown in Fig. 5, a capacitance dielectric layer 32 is formed over the patterned oxide layer 16, the bottom electrodes 30', 30'' and the bottom 28 of the capacitance trench 25 to a thickness of preferably from about 100 to 600Å and more

preferably from about 250 to 350Å. Capacitance dielectric layer 32 is preferably comprised of oxide or silicon oxide and is more preferably oxide.

Formation of Initial Via Openings 36, 38 - Fig. 6

As shown in Fig. 6, a second patterned masking layer 34 is formed over the structure of Fig. 5. Second patterned masking layer 34 includes openings 35, 37 exposing respective opposing portions of the capacitance dielectric layer 32 proximate the capacitance trench 25. Second patterned masking layer 34 is preferably comprised of photoresist as will be used for illustrative purposes hereafter.

Using second patterned photoresist layer 34 as a mask, the portions of the capacitance dielectric layer 32 exposed by the second patterned photoresist layer openings 35, 37, the underlying portions of the patterned ARC 18' and the underlying portions of the patterned oxide layer 16' down to the underlying etch stop layer 14 are removed to form respective initial via openings 36, 38. Initial via openings 36, 38 each have a width of preferably from about 0.10 to 0.50 μm and more preferably from about 0.15 to 1.46 μm .

Removal of Second Patterned Photoresist Layer 34 - Fig. 7

As shown in Fig. 7, second patterned photoresist layer 34 is removed and the structure is cleaned as necessary.

Formation of Etched-Back Third Masking Layer Portions 40, 42 - Fig. 8

As shown in Fig. 8, a third masking layer is formed over the structure of Fig. 7, filling the initial via openings 36, 38 and the capacitance dielectric layer lined capacitance trench 25, and the third masking layer is then etched back to leave portions 42 within respective initial via openings 36, 38 and portion 40 within the capacitance dielectric layer lined capacitance trench 25. Third patterned masking layer portions 40, 42 are preferably comprised of photoresist. as will be used for illustrative purposes hereafter.

Formation of Capacitance Trench Masking Portion 43 - Fig. 9

As shown in Fig. 9, a capacitance trench masking portion 43 is formed over the third patterned photoresist portion 40 within the capacitance dielectric layer lined capacitance trench 25, over portions of the patterned capacitance dielectric layer 32' adjacent the capacitance trench 25 above the respective bottom electrodes 30', 30" and over portions of the patterned capacitance dielectric layer 32' outboard of respective initial via openings 36, 38.

This leaves exposed portions 70, 72 of the patterned capacitance dielectric layer 32' between the respective initial via openings 36, 38 and the capacitance trench masking portion 43.

Capacitance trench masking portion 43 is preferably comprised of photoresist as will be used for illustrative purposes hereafter.

Formation of Trench Openings 56, 58 - Fig. 10

As shown in Fig. 10, using photoresist capacitance trench masking portion 43 as a mask, the exposed portions 70, 72 of the patterned capacitance dielectric layer 32' between the respective initial via openings 36, 38 and the capacitance trench masking portion 43, the underlying twice patterned ARC 18" and the underlying twice patterned oxide layer 16" down to a depth substantially equal to the bottom of the capacitance trench 25 to form respective trench openings 56, 58 contiguous and continuous with respective final via openings 52, 54, in turn forming respective dual damascene openings 57, 59. Final via openings 52, 54 expose underlying portions 78 of metal structure 12.

Formation of Barrier Layer 76 and Planarized Metal Portions 60, 62, 64 - Fig. 11

As shown in Fig. 11, a barrier layer 76 is formed over the structure of Fig. 10, lining the respective dual damascene openings 57, 59 and the capacitance dielectric layer lined capacitance trench 25 to a thickness of preferably from about 100 to 400Å and more preferably from about 250 to 350Å.

Barrier layer 76 is preferably comprised of TaN or TiN.

A metal layer is formed over the structure, at least filling the barrier layer 76 lined respective dual damascene openings 57, 59 and capacitance trench 25 and is then planarized to remove the excess of the metal layer overlying the barrier layer 76 lined respective dual damascene openings 57, 59 and capacitance trench 25 to form: respective planarized metal portions 62, 64 within respective dual damascene openings 57, 59; and top electrode portion 60 within capacitance trench 25 to complete formation of MIM capacitor 80.

The planarized metal portions 62, 64 and the top electrode portion 60 are preferably comprised of copper, aluminum or gold and are more preferably copper.

Further processing may then proceed. For example, as shown in Fig. 12, an inter-metal dielectric layer (IMD) 100 may be formed over the MIM capacitor 80 and a contact 102 may be formed through the IMD layer 100 to contact the MIM capacitor 80 at planarized metal portion 64.

It is noted that the method of the present invention changes the capacitor layout from horizontal to vertical at the copper (Cu) chemical mechanical process (CMP).

Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1. less planarization than previous processes for extra layer added, i.e. need extra mask photo like alignment mark open;
2. less low-k damage for low-k oxide layer 16 thickness loss during ashing and k-loss;;
3. Less MIM capacity than in conventional designs for the MIM is changed from horizontal to vertical;
4. No extra MIM define step like current, i.e. conventional MIM needs to add another mask to define the top electrode;
5. Reduced leakage problem due to etching polymer issue for polymer induce metal (top) and metal (bottom electrode); and
6. Lower cost by saving alignment mark (AM) etching and less masking.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.